9.10.2.2 PECI DC Characteristics

The PECI interface operates at a nominal voltage set by V_{CCIO}. The set of DC electrical specifications shown in Table 9-13 are used with devices normally operating from a V_{CCIO} interface supply. V_{CCIO} nominal levels will vary between processor families. All PECI devices will operate at the V_{CCIO} level determined by the processor installed in the system.

Table 9-13. PECI DC Electrical Limits

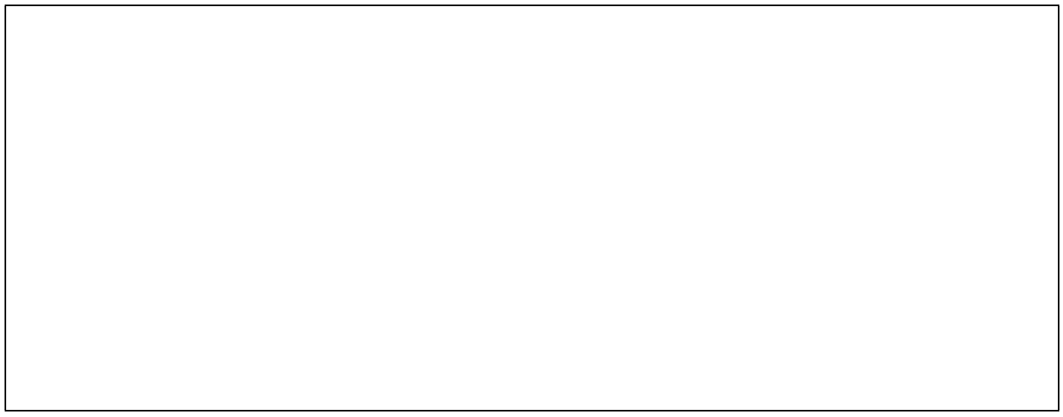
Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
Rup	Output resistance	15	45	Ohm	3
V_{in}	Input Voltage Range	-0.15	V_{CCIO}	V	
$V_{hysteresis}$	Hysteresis	0.1 * V_{CCIO}	N/A	V	
V_n	Negative-Edge Threshold Voltage	0.275 * V_{CCIO}	0.500 * V_{CCIO}	V	
V_p	Positive-Edge Threshold Voltage	0.550 * V_{CCIO}	0.725 * V_{CCIO}	V	
C_{bus}	Bus Capacitance per Node	N/A	10	pF	
C_{pad}	Pad Capacitance	0.7	1.8	pF	
Ileak000	leakage current @ 0V	-	0.6	mA	
Ileak025	leakage current @ 0.25*V_{CCIO}	-	0.4	mA	
Ileak050	leakage current @ 0.50*V_{CCIO}	-	0.2	mA	
Ileak075	leakage current @ 0.75*V_{CCIO}	-	0.13	mA	
Ileak100	leakage current @ V_{CCIO}	-	0.10	mA	

Notes:
1. V_{CCIO} supplies the PECI interface. PECI behavior does not affect V_{TT} min/max specifications.
2. The leakage specification applies to powered devices on the PECI bus.
3. The PECI buffer internal pull up resistance measured at 0.75*V_{CCIO}

9.10.2.3 Input Device Hysteresis

The input buffers in both client and host models must use a Schmitt-triggered input design for improved noise immunity. Use Figure 9-2 as a guide for input buffer design.

Figure 9-2. Input Device Hysteresis



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